Low Power Adiabatic Pfal Adder by Proper Choosing the N-Network

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Abstract: *Low Power is the main concern as the technology is reducing. Adders are the basic circuit for the arithmetic calculations. Adiabatic logics give less power dissipation than conventional CMOS. In this paper the attention is given to n-networks which can further minimize the power. The adder designed in this paper is based on the positive feedback adiabatic logic with different n-networks at 130 nm technology. Tanner EDA tool is used to design and simulate the circuits.*

***Keywords*:** *Adiabatic Adder, CMOS, Low Power, PFAL*

I. Introduction

Today digital circuits are very popular. They have a vital role in our daily life. But power dissipation is the main concern in these circuits. Power dissipation can be reduced by using the adiabatic logic over the convention CMOS logic [1]. Now adiabatic logic is divided into partially adiabatic family and fully adiabatic family. The research is mainly going on partially adiabatic logic – Efficient Charge Recovery Logic (ECRL), 2N-2N2P logic, Positive Feedback Adiabatic Logic (PFAL). But PFAL is better than others. In digital, full adder is the basic circuit for arithmetic operations. So in this paper adiabatic PFAL full adder is designed. Now how to choose n-network and /n-network so that there should be less power dissipated. It can further save more power by choosing the proper n-network.

II. Theory Of Pfal

The positive feedback adiabatic logic (PFAL) consists of latch made of two PMOS transistors and two NMOS transistors. There are two networks that are designed by only using the NMOS transistors and both networks are opposite to each other in logic. For example if NAND gate is to design using PFAL then the other network is AND gate [3], [6].

The power supply used in PFAL circuit is AC supply. It can be pulse or sinusoidal source. It is also called power clock as the output depends upon the power supply also. When it is at logic 1 then only the output comes. In the figure 1, the boxes shown are n-networks but they should be opposite in logic. It can design by using only the NMOS transistors.
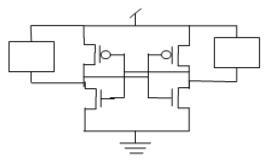

Figure 1 Basic Structure of PFAL circuit

III. Circuit Design

The design of adiabatic PFAL adder is divided into sum and carries circuits. Two sum circuits and four carry circuits are designed based on different n-networks. All the circuits are designed and simulated using Tanner EDA tools.
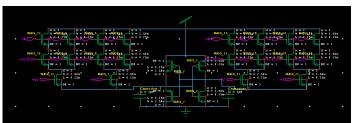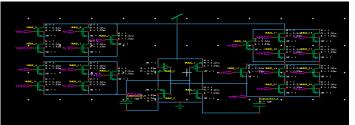

Figure 2 Sum1 circuit

Figure 3 Sum2 circuit
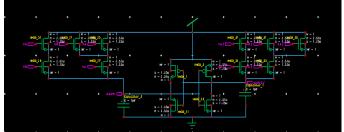

Figure 4 Carry1 circuit
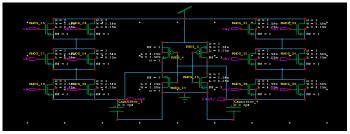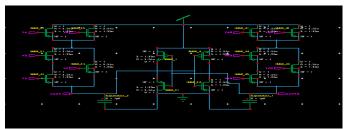

Figure 5 Carry2 circuit

Figure 6 Carry3 circuit

Figure 7 Carry4 circuit

IV. Simulation Results

The power dissipation of all the circuits calculated using Tanner EDA tools at 130nm technology. All the other parameters like threshold voltage, aspect ratio etc. is same to find out the difference in dissipation of power among all the circuits.

Combination of sum and carry circuit	Power dissipation (microwatts)
Sum1carry1	2.686
Sum1carry2	2.525
Sum1carry3	2.694
Sum1carry4	2.626
Sum2carry1	2.631
Sum2carry2	2.482
Sum2carry3	2.596
Sum2carry4	2.528

Table 1   Comparison of PFAL Adder with different n-networks

V. Conclusion

Adiabatic PFAL adder can be designed by different n-networks. Based on this, there are so many circuits but there is difference in power dissipation. From table 1, it can be seen that one can reduce the power dissipation in the adder circuit by 7.86% if sum2carry2 circuit is chosen over the sum1carry3.Sum1carry2 and sum2carry4 have almost the same power dissipation. Hence one should be careful while choosing the n-networks in adiabatic PFAL circuits so that there should be minimum power dissipation.

References

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